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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,938	06/23/2000	Joseph Herbst	108339-09032	9234

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EXAMINER	
MEW, KEVIN D	

ART UNIT	PAPER NUMBER
2664	4

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,938	HERBST, JOSEPH	
	Examiner	Art Unit	
	Kevin Mew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,16-20,22-25 and 27* is/are rejected.

7)☒ Claim(s) *13-15,21,26 and 28-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/23/2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-12, 16-20, 22-25, 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (USP 6,246,680) in view of Erimli (USP 6,061,351).

Regarding claim 1, Muller discloses a network switch (switch element, see lines 45-46, col. 2 and Fig. 3) comprising:

at least one port data port interface (Bus Interface, see element 340, Fig. 3);

a first memory (Pointer RAM, see element 320, Fig. 3);

a second memory (Shared Memory, see element 230, Fig. 3); and

a memory management unit (shared memory manager that manages input and output Ethernet packets, see lines 53-58, col. 5 and element 220, Fig. 3) in connection-with said at least one data port interface (Bus IF, see element 340, Fig. 3), said first memory (the Pointer RAM, see element 320, Fig. 3), and said second memory (see Shared Memory, see element 230, Fig. 3),

wherein the memory management unit (shared memory manager that manages input and output Ethernet packets, see lines 53-58, col. 5 and element 220, Fig. 3) receives data from the at least one data port interface (shared memory manager provides an efficient centralized interface to the share memory 230 for buffering of incoming packets from the Bus Interface, see lines 49-51, col. 7), determines if the data is to be

stored in one of the first memory or the second memory (the IPPs temporarily store the packet data in the shared memory until a forwarding decision is received from the switch fabric, see lines 51-58, col. 5), retrieves the data from one of the first memory or the second memory (the shared memory manager comprises buffer memory controller that stores and retrieves packet data to the shared memory 230, see lines 21-22-25, col. 8), and forwards the data for egress (the shared memory manager retrieves packet from the external shared memory to be forwarded to the output ports, see lines 31-35, col. 5).

Muller does not explicitly disclose storing the data in one of the first memory or the second memory as a linked list. However, Erimli discloses a network switch wherein frame data received from any PCI bus is stored in external memory in a linked-list data structure format. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the storage structure format of the external memory of Muller with the linked-list structure format of the external memory of Erimli. The motivation to do so is to provide an efficient data insertion and retrieval because it is well known in the art that linked-list allows the list to traverse from start to end quickly.

Regarding claim 2, Muller discloses a network switch as recited in claim 1, said network switch further comprising

a status location budget manager (shared memory manager, see element 220, Figs. 2 and 3) in connection with the at least one data port interface, the first memory, and the second memory, for determining if the data is to be stored in the first memory or the second memory (interfaces with every input port and output port and performs dynamic memory allocation and deallocation on their behalf, see lines 24-26, col. 5).

Regarding claim 3, Muller discloses a network switch as recited in claim 1, said network switch further comprising

a first memory controller (buffer manager, see element 325, Fig. 3) for storing data within said first memory (Pointer RAM, see lines 9-13, col. 8 and element 320, Fig. 3) and a second memory controller (buffer memory controller, see element 330, Fig. 3) for storing data within said second memory (Shared Memory, see lines 22-25, col. 8 and element 230, Fig. 3).

Regarding claim 4, Muller discloses a network switch as recited in claim 1, wherein said first memory further comprises on-chip memory (see Pointer RAM is a ob-chip pointer table that is inside the switch element and lines 46-47, col. 2, lines 11-13, col. 8 and Fig. 3).

Regarding claim 5, Muller discloses a network switch as recited in claim 1, wherein said second memory further comprises off-chip memory (see Shared Memory is outside the switch element and lines 46-47, col. 2 and Fig. 3).

Regarding claim 6, Muller discloses a network switch as recited in claim 1, wherein the memory management unit (the unit that comprises shared memory manager, switch fabric, buffer manager, pointer RAM, buffer memory controller and shared memory, see elements 210, 220, 230, 320, 325, 330, Fig. 3) further comprises

a communication channel (communication channels formed by coupling input ports to the output ports, see lines 11-16, col. 5);

a data input section (section comprising Bus IF, Shared Memory Manager, IPPs, Switch Fabric, see elements 340, 220, 310-312, 210, Fig. 3) in connection with the communication channel;

a data output section (section comprising Host Receive Process, Shared Memory Manager, OPPs, see lines 41-45, col. 4 and elements 360, 220, 315-317, Fig. 3) in connection with the communication channel;

a first memory controller (Buffer Manager, see element 325, Fig. 3) in connection with the first memory (pointer RAM, see element 320, Fig. 3), the data input section (section comprising Bus IF, Shared Memory Manager, IPPs, Switch Fabric, see elements 340, 220, 310-312, 210, Fig. 3), and the data output section (Buffer Manager in connection with Pointer RAM, Bus IF and network interface, see elements 325, 340, and 205, Fig. 3);

a second memory controller in connection with the second memory, the data input section, and the data output section (Buffer Memory Controller in connection with Shared Memory, Bus IF and network interface, see elements 330, 230 and 205, Fig. 3);

at least one address pool (shared memory is a pool of buffers, see lines 49-57, col. 7 and element 230, Fig. 3) in connection with the first memory controller (see element 325, Fig. 3) and the second memory controller (see element 330, Fig. 3); and

a scheduler (shared memory manager, see element 220, Fig. 3) in connection with the data input section (section that comprises Bus IF 340, Switch Fabric 210, Shared Memory Manager 220, IPPs 310-312, see Fig. 3) and the data output section (section

comprising Host Receive Process, Shared Memory Manager, OPPs, see lines 41-45, col. 4 and elements 360, 220, 315-317, Fig. 3).

Regarding claim 7, Muller discloses a network switch as recited in claim 6, wherein the data input section further comprises:

a cell assembly unit (switch fabric includes new MAC destination address, processes packet headers and adds priority indication to facilitate prioritization of packet traffic, see lines 16-21, element 210, Fig. 3) in connection with the communication channel (communication channels formed by coupling input ports to the output ports, see lines 11-16, col. 5);

a status location budget manager (shared memory manager, see element 220, Figs. 2 and 3) in connection with the cell assembly unit(switch fabric, see element 210, Fig. 3) ;

at least one cell accumulation buffer (IPPs, see elements 310-312, Fig. 3) in connection with the status location budget manager (shared memory manager, see element 220, Figs. 2 and 3);

a slot assembly unit (network interface, see lines 45-52, col. 4 and element 205, Fig. 3; note that the network interface modifies incoming packet headers as appropriate and transfers incoming packet data to the shared memory manager for temporary storage in an external shared memory) in connection with the at least one cell accumulation buffer (IPPs, see elements 310-312, Fig. 3) and said second memory controller (shared memory, see element 230, Fig. 3); and

at least one address pool (shared memory, see element 230, Fig. 3) in connection with the status location budget manager (shared memory manager performs dynamic memory allocation of input port buffers, see lines 25-27, col. 5 and element 220, Figs. 2 and 3), the slot assembly unit (network interface, see element 205, Fig. 3) and the data output section (OPPs, Shared Memory Manager, Host Receive Process, see elements 315-317, 220, 360, Fig. 3).

Regarding claim 8, Muller discloses a network switch as recited in claim 7, wherein the cell assembly unit converts data received from the communication channel into a cell header format (see lines 16-19, col. 5), a cell data format (see lines 11-21, col.. 5), and a sideband information format (see lines 19-21, col. 5).

Regarding claim 9, Muller discloses a network switch as recited in claim 7, wherein the status location budget manager determines whether data received by the cell accumulation buffer is to be stored in the first memory or the second memory (shared memory manager allocates dynamic memory buffers on bin the external shared memory on half of the input ports, see lines 24-28, col. 5).

Regarding claim 10, Muller discloses a network switch as recited in claim 7, wherein the at least one cell accumulation buffer collects data (IPPs, see elements 310-312, Fig. 3) to be stored in the second memory prior to sending the data to be stored in the second memory to the slot assembly unit (network interface, see element 205, Fig. 3).

Regarding claim 11, Muller discloses a network switch as recited in claim 7, wherein the slot assembly unit (network interface, see element 205, Fig. 3) receives cells from the cell accumulation buffer and packages the received cells into cell slots to be stored in the second memory (see lines 45-52, col. 4).

Regarding claim 12, Muller discloses a network switch as recited in claim 6, wherein the data output section further comprises:

a cell disassembly unit (Host Receive Process HRP, see element 360, Fig. 3) in communication with the communication channel (communication channels formed by coupling input ports to the output ports, see lines 11-16, col. 5);

a cell retrieval and reclaim unit (shared memory manager retrieves packets from shared memory 230 and deallocates buffers that are no longer in use, see lines 32-35, col. 5 and element 220, Fig. 3) in communication with the cell disassembly unit (Host Receive Process HRP, see element 360, Fig. 3); and

a read buffer (shared memory, see element 230, Fig. 3) and slot disassembly unit (Host Receive Process HRP, see element 360, Fig. 3) in communication with the cell retrieval and reclaim unit (shared memory manager) and the second memory controller (shared memory manager retrieves packets from shared memory 230 via the buffer memory controller and deallocates buffers that are no longer in use, see lines 32-35, col. 5, and lines 21-24, col. 8 and element 220, Fig. 3).

Regarding claim 16, Muller discloses a network switch as recited in claim 12, wherein the read buffer (OPPs, see element 315-317, Fig. 3) and slot disassembly unit reads slots from the second memory (HRP retrieves the packet from the external shared memory, see lines 31-36, col. 5) and sends the slots to the first memory (on-chip memory 320 stores counts of buffers of the shared memory 230).

Regarding claim 17, Muller discloses a network switch as recited in claim 7, wherein said at least one address pool further comprises

a cell free address pool (pointer RAM, see element 320, Fig. 3), see elements 310-312, Fig. 3) connected to the first memory controller (buffer manager, see element 325, Fig. 3); and

a slot free address pool (shared memory, see element 230, Fig. 3) connected to the second memory controller (Buffer Memory Controller, see element 330, Fig. 3).

Regarding claim 18, Muller discloses a network switch as recited in claim 6, said network switch further comprising:

a cell free address pool unit (pointer RAM, see element 320, Fig. 3) connected to the first memory controller (buffer manager, see element 325, Fig. 3);

a slot free address pool unit (shared memory, see element 230, Fig. 3) connected to the second memory controller (buffer memory controller, see element 330, Fig. 3); and

a scheduler (shared memory manager, see element 220, Fig. 3) connected to the first memory controller (buffer manager, see element 325, Fig. 3) and the second memory controller (buffer memory controller, see element 330, Fig. 3).

Regarding claim 19, Muller discloses a network switch as recited in claim 18, wherein the cell free address pool unit (pointer RAM, see elements 310-312, Fig. 3) further comprises a cell free address pool (dynamically allocated buffers, see lines 24-28, col. 5) and a cell free address pool controller (shared memory manager, see element 220, Fig. 3) connected to the cell free address pool (dynamically allocated buffers, see lines 24-28, col. 5).

Regarding claim 20, Muller discloses a network switch as recited in claim 19, wherein the cell free address pool controller (shared memory manager, see element 220, fig. 3) is configured to receive and release free addresses from the cell free address pool unit for use in storing cells in the first memory (see lines 24-28, col. 5).

Regarding claim 22, Muller discloses a network switch as recited in claim 18, wherein the slot free address pool unit (shared memory 230, Fig. 3) further comprises a slot free address pool (dynamically allocated buffers) and a slot free address pool controller (buffer memory controller, see element 330, Fig. 3) connected to the slot free address pool (dynamically allocated buffers, see lines 24-28, col. 5).

Regarding claim 23, Muller discloses a network switch as recited in claim 22, wherein the slot free address pool controller is configured to receive and release free slots from the slot free address pool for use in storing cells in the second memory (see lines 24-28, col. 5).

Regarding claim 24, Muller discloses a network switch as recited in claim 18, wherein the first memory controller receives and processes requests for storage of data in the first memory (see lines 9-15, col. 8 and element 325, Fig. 3).

Regarding claim 25, Muller discloses a network switch as recited in claim 18, wherein the second memory controller receives and processes requests for storage of data in the second memory (see lines 21-24, col. 8 and element 330, Fig. 3).

Regarding claim 27, Muller discloses a method for storing data in a network switch, said method comprising the steps of:

receiving data to be transmitted to an egress at an input to a memory management unit (the unit that comprises shared memory manager, switch fabric, buffer manager, pointer RAM, buffer memory controller and shared memory, see elements 210, 220, 230, 320, 325, 330, Fig. 3);

determining if the data is to be stored in a first memory or a second; and storing the data in the first memory or the second memory based on the determining step memory (the IPPs temporarily store the packet data in the shared memory until a forwarding decision is received from the switch fabric and the OPPs retrieve packet data from the shared memory when a packet is ready for transmission, see lines 51-58, col. 5).

Muller does not explicitly disclose formatting the data received as a linked list. However, Erimli discloses a network switch wherein frame data received from any PCI bus is stored in external memory in a linked-list data structure format. Therefore, it

would have been obvious to one ordinary skill in the art at the time the invention was made to modify the storage structure format of the external memory of Muller with the linked-list structure format of the external memory of Erimli. The motivation to do so is to provide an efficient data insertion and retrieval because it is well known in the art that linked-list allows the list to traverse from start to end quickly.

Allowable Subject Matter

2. Claims 13-15, 21, 26, 28-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In claim 13, a network switch as recited in claim 12, wherein the cell disassembly unit converts a cell format from a CBP format to a CP bus format and transmits a cell to the communication channel when enabled to do so.

In claim 14, a network switch as recited in claim 12, wherein the cell retrieval and reclaim unit receives egress for cells and schedules cell egresses through the cell disassembly unit in accordance with a predetermined algorithm.

In claim 15, a network switch as recited in claim 14, wherein the predetermined algorithm further comprises a token order.

In claim 21, a network switch as recited in claim 18, wherein the scheduler transmits a token between at least two egress managers in accordance with a predetermined algorithm, thereby allowing the at least two egress managers to individually schedule an egress transmission of data when the token is present.

In claim 26, a network switch as recited in claim 25, wherein the second memory controller receives requests from a slot assembly unit, the slot free address pool, a slot assembly unit, and a refresh requestor.

In claim 28, a method for storing data in a network switch as recited in claim 27, wherein the determining step further comprises the steps of:

determining if a cell count is less than a first predetermined threshold for the egress;

determining if a number of cells in the second memory is zero; and

determining if a number of cells in the first memory added to a number of cells remaining in an assembly is less than the first predetermined threshold.

In claim 29, a method for storing data in a network switch as recited in claim 27, wherein the step of storing data in the first memory further comprises the steps of:

initializing a cell count;

setting an in progress flag;

loading a first cell pointer into a memory controller;

incrementing the cell count;

storing a first cell in the local memory;.

In claim 31, a method for storing data in a network switch as recited in claim 27, wherein

the step of storing data in the second memory further comprises the steps of initializing global storage of data and continuing global storage of data until a last slot is stored.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure with respect to memory management unit in a network switch.

US Patent 5,841,771 to Irwin et al.

US Patent 5,412,655 to Yamada et al.

US Patent 5,844,906 to Khelghatti et al.

US Patent 5,255,264 to Cotton et al.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 703-305-5300. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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